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VHDL Design of OFDM Transreceiver Chip using Variable FFT

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ABSTRACT

Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier transmission technique that divides the available spectrum into multiple carriers in which each one is being modulated by a low rate data stream. OFDM is similar to FDMA in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels band, which is then allocated to users. So, OFDM uses the spectrum much more efficiently by spacing the channels much closer together. It is possible by making all the carriers orthogonal to each another, preventing interference between the closely spaced carriers. The research is relating to the design and synthesis of variable input FFT processor which is designed to meet the requirements of OFDM & OFDMA system. The FFT and IFFT pairs are used to modulate and demodulate the data constellation on the subcarriers in OFDM and OFDMA. The research presents a high level implementation of a high performance FFT for OFDM Demodulator. The work is carried out on Xilinx 14.2 software and functional checked in Modelsim 10.1b software. The language used for the design in VHDL.

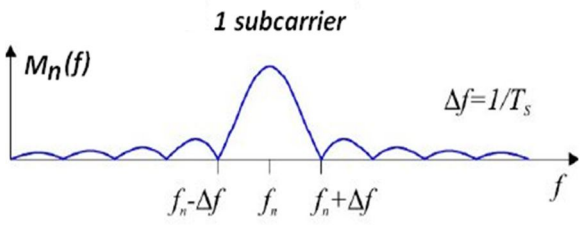
Keywords- Orthogonal Frequency Division Multiplexing (OFDM), Fast Fourier Transform (FFT), Inverse Fast Fourier Transform (IFFT), Very Large Scale of Integration (VLSI), Hardware Description language (HDL)

I.INTRODUCTION

With the rapid growth of digital communication in recent years, there is the need for high-speed data transmission with faster rate. The mobile telecommunication industries are facing the problem of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Couple of systems have been proposed to resolve the problem and OFDM system has gained much attention for different reasons. OFDM [1] [2] technique was first developed in the 1960s. Only in recent years, OFDM has been recognized as an outstanding method for high speed cellular data communication where its

implementation relies on very high speed digital signal processing applications. The method has only recently become available with reasonable prices versus performance of hardware implementation. Since OFDM is carried out in the digital domain. Hence, there are several methods to implement the systems based on the technology. One of the methods to implement the system is using Field-Programmable Gate Array (FPGA).This hardware is programmable and the designer has full control over the actual design implementation without the need for any physical IC fabrication facility. An FPGA module combines the power, speed, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA [12] could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. It will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others **OFDMA.**

The technique of orthogonal frequency division multiplexing (OFDM) is used in many wired and wireless communication systems. In general, the Fast Fourier Transform (FFT) and inverse FFT (IFFT) operations are used as the demodulation /modulation in the OFDM systems. The sizes of FFT/IFFT [3] [4] operations are varied in different applications of OFDM systems. OFDM is especially suitable for high-speed communication due to its resistance to ISI. A communication system increases its information transfer speed and time for each transmission necessarily becomes shorter. ISI becomes a limitation in high data rate communication, although the delay time caused by multipath remains constant. The orthogonal nature of all carriers in OFDM leads the faster communication of data. OFDM technology uses the multicarrier. The single carrier signal is shown in figure 1(a) and multicarrier concepts and their representation for OFDM are shown in figure 1 (b) respectively, in which 6 multicarrier are represented by their orthogonal nature, having frequencies f_1, f_2, f_3, f_4, f_4, f_5 and f_6 respectively.



(a) Single carrier

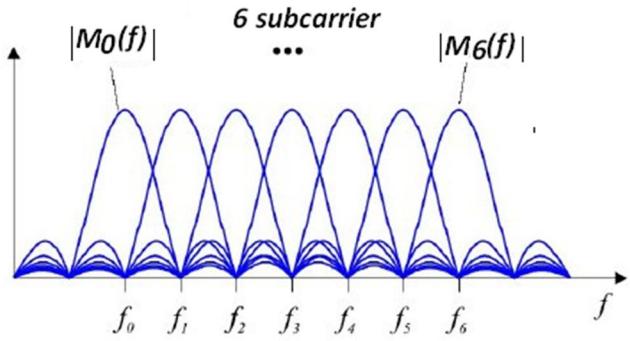


Fig. 1 (b) OFDM representation

The related work is discussed with the help of some research papers. The research paper [3] explains how design and implementation of Fast Fourier Transform (FFT) algorithm is done for wireless-communication and its applications in real time environment. VHDL language is used in this algorithm, which is functional verified and simulated in the MODEL SIM SE tool, that provides new methodology to design and develop the processor for the Digital Signal processing aspects, and is implemented on the basis of pipelined architecture and Fast Fourier Transform approach. The computational scheme is two dimensional and implementation of this scheme on VIRTEX 5 LX330 FF1145 based XILINX's FPGA. In paper [4] they have introduced a memory based recursive FFT design which has much less gate counts, lower power consumption and higher speed. The technology provides up to 10 Mbps broadband speed without the need for cables. The technology on which they worked is based on the IEEE 802.16 standard also called Broadband Wireless Access. The 802.16e standard is extended for OFDMA with 2K-FFT, 512-FFT, 1K-FFT and 256-FFT capability. The FFT algorithm eliminates the redundant calculation which is needed in computing Discrete Fourier Transform (DFT) and is thus very suitable for efficient hardware implementation. Radix -22 hardware based algorithm is developed by integrating a twiddle factor decomposition technique in divide and conquer approach to form a spatially regular Signal Flow Graph (SFG). Linear filtering is also done to computing efficient DFT and FFT a applications in correlation analysis and digital spectral analysis, and Ultra Wide Band (UWB) applications, etc. 8-point IFFT & FFT algorithms [10] using VHDL are implemented in the 802.11a architecture of OFDM transmitter & receiver.

The performance of the main processing block of OFDM transceiver is upgraded by reducing the clock cycles in their above work. OFDM system based on IEEE 802.11 is an standard for WLAN. This system consists of separate OFDM transmitter & receiver and entire module is implemented using implemented FFT and IFFT blocks in VHDL. The speed Enhancement is the achieved of the main processing blocks in OFDM system. In another paper [12], an 8-point FFT module is the kernel part of the architecture which consists of butterfly structure, weight functions as twiddle factor, coefficient RAM, controller and an address generation unit. The results of the 8-point FFT module are compared with MATLAB results. Pipelined structure is implemented.

I. FFT & IFFT TRANSFORM

The Inverse fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) and are used in OFDM and OFDMA [10] transmitter and receiver to modulate and demodulate the data.

2.1 Fast Fourier Transform

The fast Fourier Transform (FFT) is a discrete transform that efficiently computes the discrete Fourier Transform (DFT). The DFT of sequence x(n) over length N is given by the relation which is a complex valued sequence X(k).

$$( ) = \quad ( ) \quad \text{——},$$

$$h \quad 0 \leq \leq \quad -1 \qquad (1)$$

The equation can be represented by the relation

$$( ) = \quad ( ) \quad / = \quad ( ) \quad ,$$

$$h \quad 0 \leq \leq \quad -1 \qquad (2)$$

Here W_N represents the complex valued phase factor, which is the N^{th} root of unity and expressed as $= \quad /$

Similarly the equation of IDFT is given as

$$( ) = \frac{1}{} \quad ( ) \qquad h \quad 0 \leq$$

$$\leq \quad -1 \qquad (3)$$

From the above equations it is clear that for each value of k, the direct computation of X(k) require N complex multiplications (4N real multiplications and N-1 complex additions(4N-2 real additions). Hence to compute all N values of DFT, there is the requirement of N^2 complex multiplications and N (N-1) complex additions.

To compute the N point DFT, the equation is given by

$$( ) = \quad ( ) + \quad ( )$$

$$( ) = \quad ( ) + \quad ( ) \quad \frac{2}{\text{——}} - \quad \frac{2}{\text{——}}$$

Where x(n) is a complex valued sequence, and X_R and X_I represents the real and imaginary parts. If we equate the real and imaginary parts separately, the above equation will be given by

$$( ) = \quad ( ) \quad \frac{2}{\text{——}}$$

$$+ \quad ( ) \quad \frac{2}{\text{——}} \qquad (4)$$

$$( ) = - \quad ( ) \quad \frac{2}{\text{——}}$$

$$- \quad ( ) \quad \frac{2}{\text{——}} \qquad (5)$$

There is the requirement of $2N^2$ Trigonometric evaluations to compute DFT directly.$4N^2$ real multiplications and 4N (N-1) real additions. It is primarily inefficient as it does not exploit the periodicity and symmetry properties of Weight function or phase factor $W_{N,}$ which is given by

$$h$$

$$/ = - \qquad (6)$$

$$h$$

$$= \qquad (7)$$

The solution of the two properties of DFT is the fast Fourier transform (FFT), which is an efficient algorithm can exploit the above two equations.

2.2 Inverse Fast Fourier Transform

An FFT algorithm for determining the inverse fast Fourier transform (IFFT) is readily obtained from FFT algorithm. It is using the lies in transforming spectra into the corresponding waveforms values and checks weather FFT has been computed correctly by the same algorithm to obtain the original data.

$$( ) = \frac{1}{} \quad ( )$$

$$= 0,1,2, \ldots \quad -1 \qquad (8)$$

Taking complex conjugate of the above equation,

$$*$$

$$= \quad *( ) \qquad (9)$$

Right hand side is the DFT computed for the sequence $*( )$. Therefore,

$$^{*}( ) = \frac{1}{} \text{DFT}[\ ^{*}( )] \quad (10)$$

Taking the complex conjugate of both sides, the desired output sequence x(n) can be written as

$$( ) = \frac{1}{} \ ^{*}( ) \quad (11)$$

Hence,

$$( ) = \frac{1}{} (\text{FFT}[X^{*}(k)])^{*}$$

2.3 SIMULATION MODEL OF OFDM

In OFDM transmission technique, the available spectrum is divided into many carriers, each carrier is being modulated by a low rate data stream. OFDM is similar to FDMA in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels, later these are allocated to users. OFDM technique uses the available spectrum much more efficiently by spacing the channels much closer together by making all the carriers orthogonal to each another. Orthogonal nature of carriers prevents interference between the closely spaced carriers. To generate OFDM this care is taken care adopting the modulation scheme. Each carrier is associated with the data to transmit. The phase and amplitude is calculated using any modulation technique QPSK, differential BPSK or QAM. Then Inverse Fast Fourier Transform (IFFT) is used to convert the frequency signal to time domain signal. IFFT is an efficient transform to ensure the converted signals are orthogonal. The Fast Fourier Transform (FFT) transform is used to convert cyclic time domain signal into its equivalent frequency spectrum. This is possible by finding the equivalent waveform, generated by a sum of orthogonal sinusoidal components. The frequency spectrum of the time domain signal is presented by the amplitude and phase of the sinusoidal components. The IFFT performs the reverse application to transform a spectrum amplitude and phase of each component into a time domain signal. Time domain signal of the same number of points of length that is a power of 2 are converted with the help of IFFT and number of complex data points. The data point present in FFT and IFFT spectrum is called a bin. The orthogonal carriers of OFDM are generated with help of setting the frequency and phase of each bin and then perform IFFT. The reverse process guarantees that the carriers generated are orthogonal because each bin of an IFFT corresponds to the amplitude and phase of a set of orthogonal sinusoids in FFT.

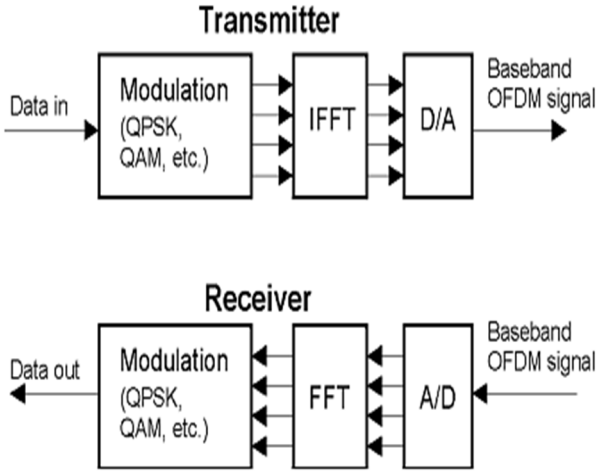


Fig. 2 OFDM transmitter and receiver

The simulation block diagram of OFDM is shown in figure 3. OFDM transmission part has serial data as input data which is converted into parallel form and mapped as the input of IFFT in OFDM modulator. The parallel output of OFDM modulator is converted to serial form and passed through AWGN channel. The output of AWGN [13] is also in serial form which again converted to parallel form and given as input to FFT in demodulator. The parallel of FFT demodulator is demapped as serial output data on receiving end. The block diagram can be understood with the help of this example. For example, Let the data input is of 64 bits ***CTK Univ***. In the data ***CTK Univ***, each character has its equivalent 8 bits ASCII code which can be seen the ASCII table. 64 bit data in binary is (**01000011** 01010100 **01001011** 00100000 **01010101 01101110 01101001 01110110)** which is mapped or converted from serial data to parallel data into its equivalent 8 bit ASCII code for each character as listed in table 1. This input data of 8 point IFFT module may be complex number. Hence, there is the requirement to present complex (real and imaginary) numbers in binary. 32 bit and 64 floating point conversion is used to present real or complex numbers. That's why the input and output of IFFT and FFT are considered of 32 bits as shown in table 2. The output of FFT is in parallel form and converted again to serial data to send over AWGN channel and again converted to parallel form of 32 bits inputs of 8-point FFT. FFT output is demapped according to 8 bits ASCII code values which give the

actual input data. The demapped data for the discussed problem is listed in table 3

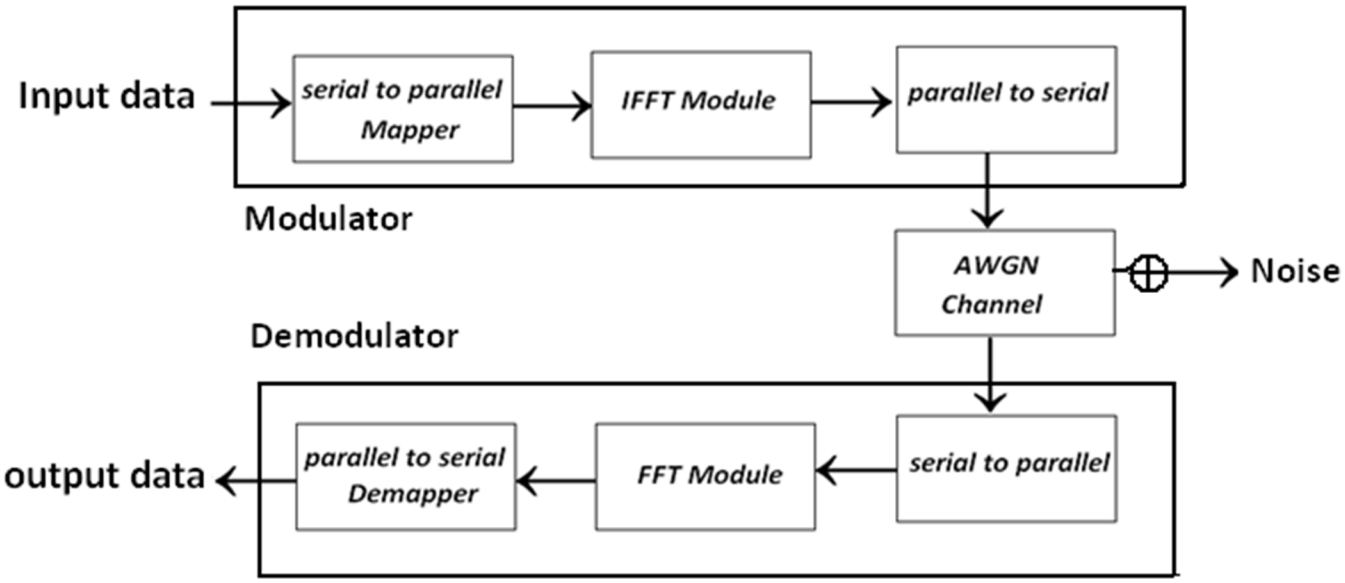


Fig. 3 Functional block diagram of OFDM (data transfer scheme)

Table 1 input data sequence to OFDM Module

Serial input data = CTK Univ (64 bits)			
01000011 01010100 **01001011** 00100000 **01010101 01101110 01101001 01110110 (Binary)** **C T K U n i v (data in)**			
Character	**Hex code**	**Decimal value**	**Equivalent Binary number**
C = one character = 8 bits	43	67	01000011
T = one character = 8 bits	54	84	01010100
K = one character = 8 bits	4B	75	01001011
Space = one character = 8 bits	20	32	00100000
U = one character = 8 bits	55	85	01010101
n = one character = 8 bits	6E	110	01101110
i = one character = 8 bits	69	105	01101001
v = one character = 8 bits	76	118	01110110

Table 2 Mapped data stream to IFFT module

Input data	**8 bits ASCII code (Mapper)**	**32 bits input for IFFT**	**Output of IFFT**
C	01000011	00000000000000000000000001000011	Output of IFFT modulator (32 bits) is the input of FFT demodulator. Let Y(0).....Y(7) are inputs and X(0).....X(7) are corresponding outputs of IFFT, then FFT inputs are X(0).....X(7).
T	01010100	00000000000000000000000001010100	
K	01001011	00000000000000000000000001001011	
	00100000	00000000000000000000000000100000	
U	01010101	00000000000000000000000001010101	
n	01101110	00000000000000000000000001101110	
i	01101001	00000000000000000000000001101001	
v	01110110	00000000000000000000000001110110	

Table 3 Demapped data stream after FFT module

Input of FFT	32 bits output for FFT	8 bits code (Demapper)	Output data
Output of IFFT modulator (32 bits) is the input of FFT demodulator. Let X(0).....X(7) are inputs of FFT and Y(0)..... Y(7) are corresponding outputs of FFT.	00000000000000000000001000011	01000011	C
	00000000000000000000001010100	01010100	T
	00000000000000000000001001011	01001011	K
	00000000000000000000000100000	00100000	
	00000000000000000000001010101	01010101	U
	00000000000000000000001101110	01101110	n
	00000000000000000000001101001	01101001	i
	00000000000000000000001110110	01110110	v

Table 4 Selection logic for FFT

Selection logic (S_2 S_1 S_0)	FFT selection
000	Module FFT0 is selected
001	Module FFT1 is selected
010	Module FFT2 is selected
011	Module FFT3 is selected
100	Module FFT4 is selected
101	Module FFT5 is selected
110	Module FFT6 is selected
111	Module FFT7 is selected

In OFDMA multiple access techniques are used in which more than one 8 point FFT and IFFT are used in modulator and demodulator. Sometime if the transmitted data is large there is the requirement to use more than one 8 point FFT/IFFT. Figure 4(a) and 4(b) shows the input and output logic of FFT and IFFT respectively. The design of multiple accesses is done using pipeline and parallel algorithm as shown in figure 4, in which designing of 'N' point variable FFT is possible. Let N = 64, to realize 64 point FFT , we have to use eight, 8-point FFTs in parallel and to synchronize all FFTs there is selection logic by which we can choose the particular FFT and analyze the corresponding FFT output as well as the output of all 64 points. Similarly it is possible to increase the size of FFT/IFFT in terms of 'N' points also depends on the particular application.

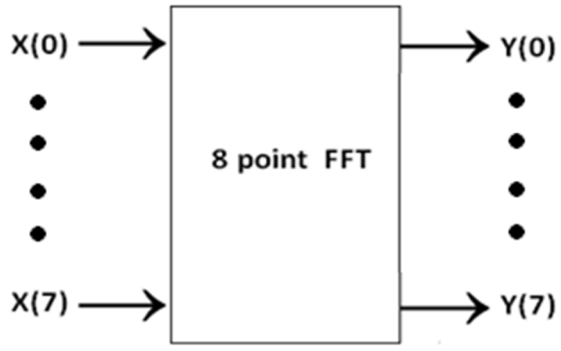


Fig. 4(a) Input and output of FFT logic

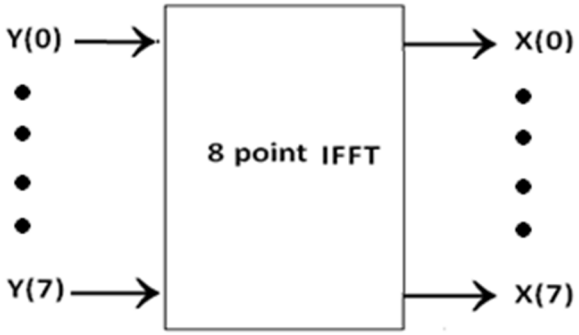
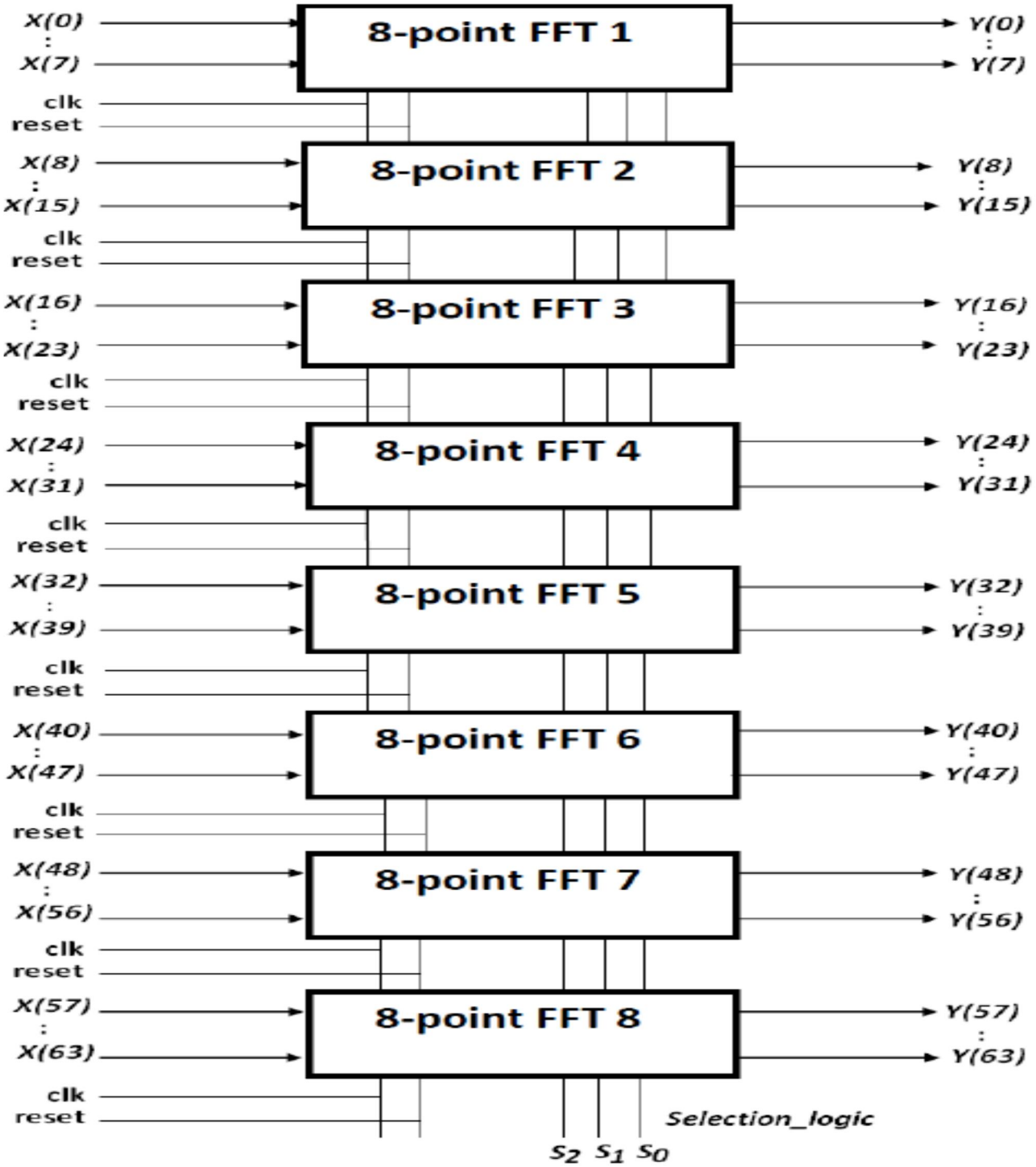


Fig. 4 (b) Input and output of IFFT logic

The selection of 64 point FFTs depends on the selection logic input which is of 3 bits. Each possible selection bits presents the selection of one 8-point FFT. Table 4 presents the selection scheme of 8 FFTs used to implement 64 point FFT. When selection logic is 000, FFT0 is selected, when selection logic is 001, FFT1 is selected and so on. Similarly when selection logic is 111, FFT7 is selected.



II. RESULTS & DISCUSSION

The Modelsim output of OFDM Transreceiver with 8 point FFT and 64 point FFT are shown in figure 6(a) and 6(b) respectively. The flow diagram of functional simulation is shown in figure 7. In the diagram X(0)..... X(7) presents the input to FFT module and Y(0)....Y(7) presents the output of 8-point FFT module. In transreceiver

Y(0)....Y(7) presents the input of IFFT and output of FFT, X(0).....X(7) presents the input of FFT and output of IFFT. In the 64 bit FFT simulation output, X(0).....X(63) presents the inputs and Y(0) ..... Y(63) presents the corresponding outputs with real and imaginary

components. Functional simulation depends on the following step inputs.

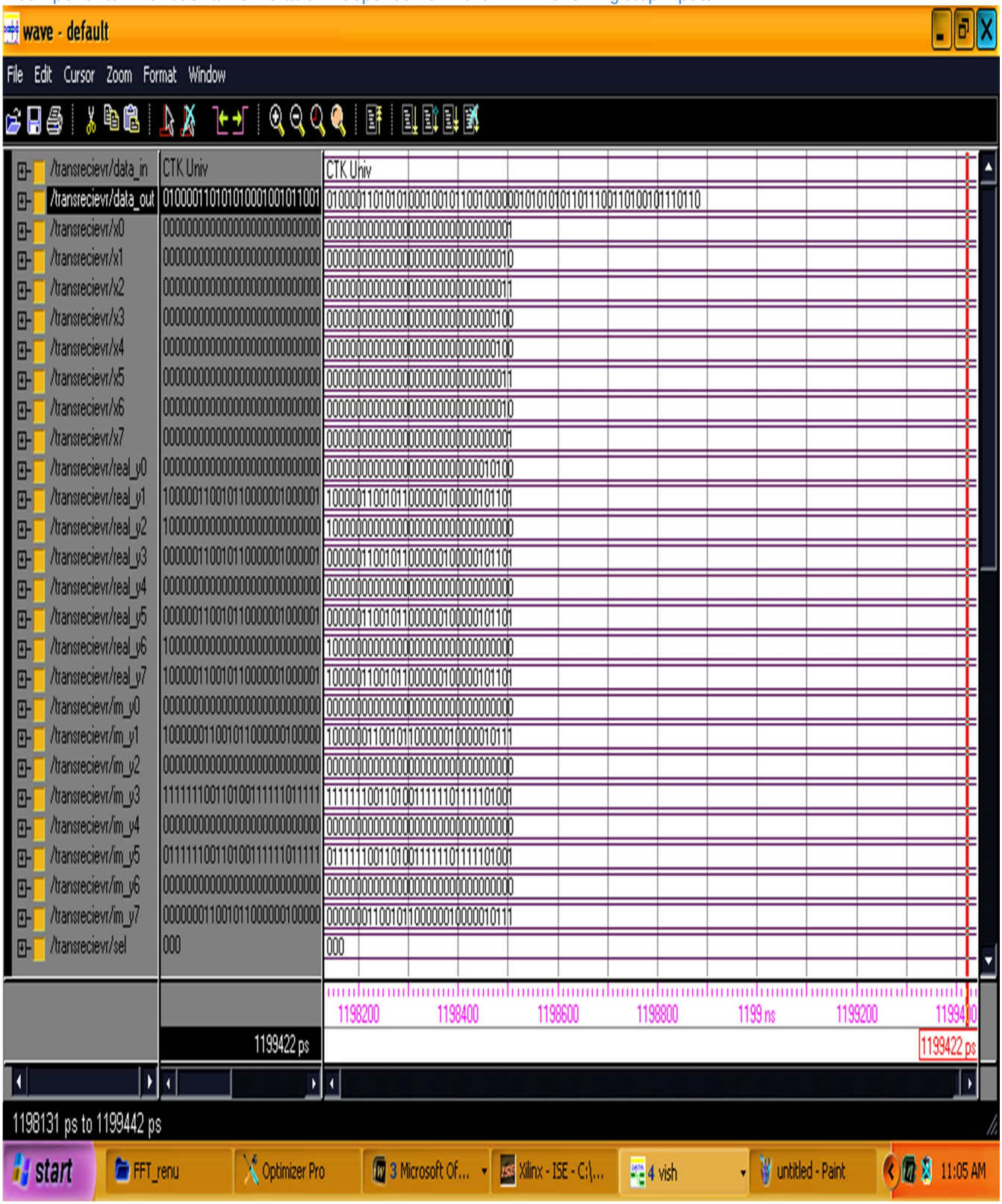


Fig. 6(a) Modelsim output of Transreceiver with 8-point FFT

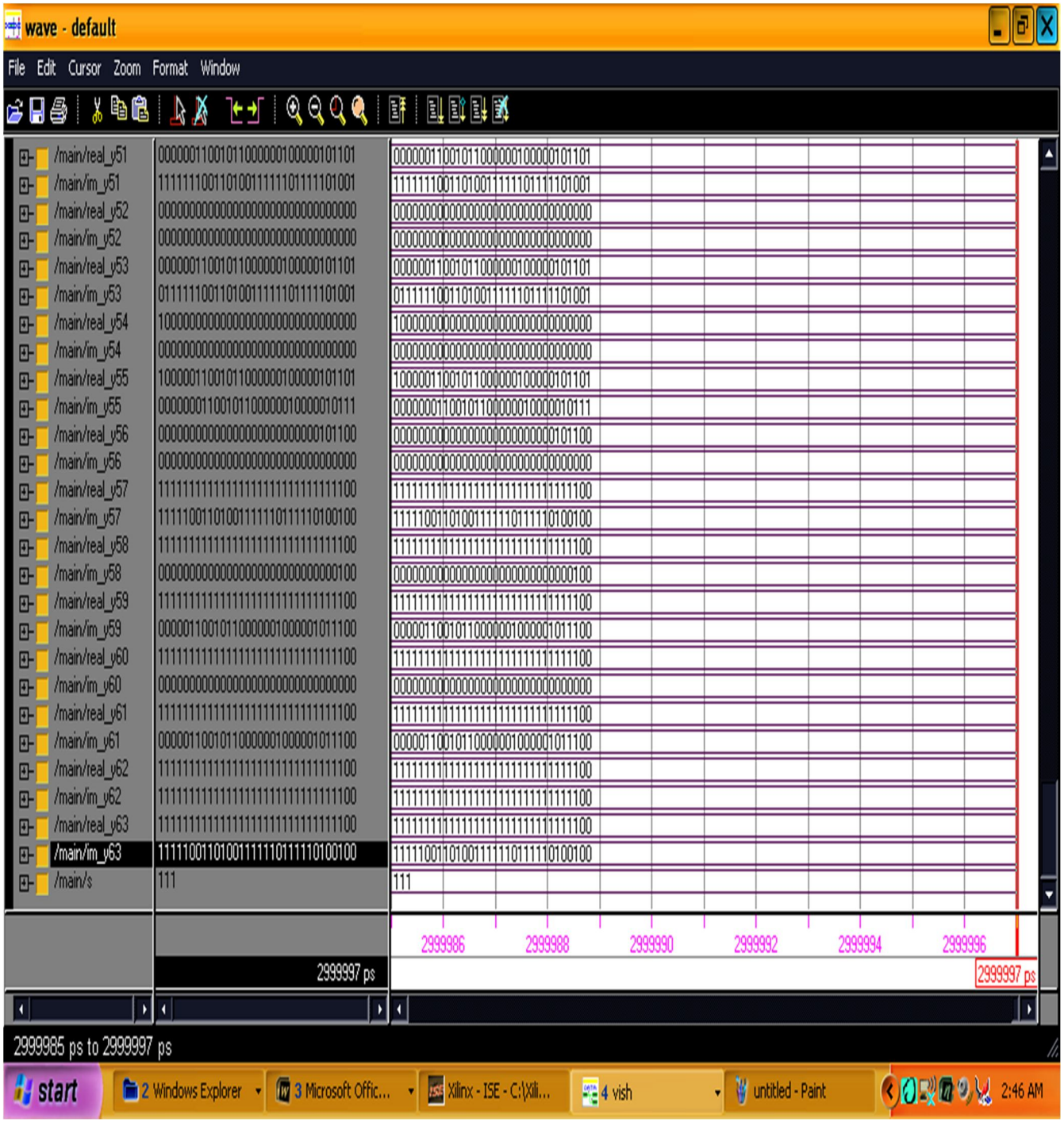


Fig 6(b) Modelsim output of FFT 64

Input Logic 1: Force the value of data_in and X(0) to X(7) and run

Input logic 2: The output of FFT and input of FFT Y(0).... Y(7) are in separated in real and imaginary parts because the output of FFT may be a complex number real_Y(0)..... real_Y(7) are the real parts and im_Y(0).....im_Y(7) are imaginary parts of output.

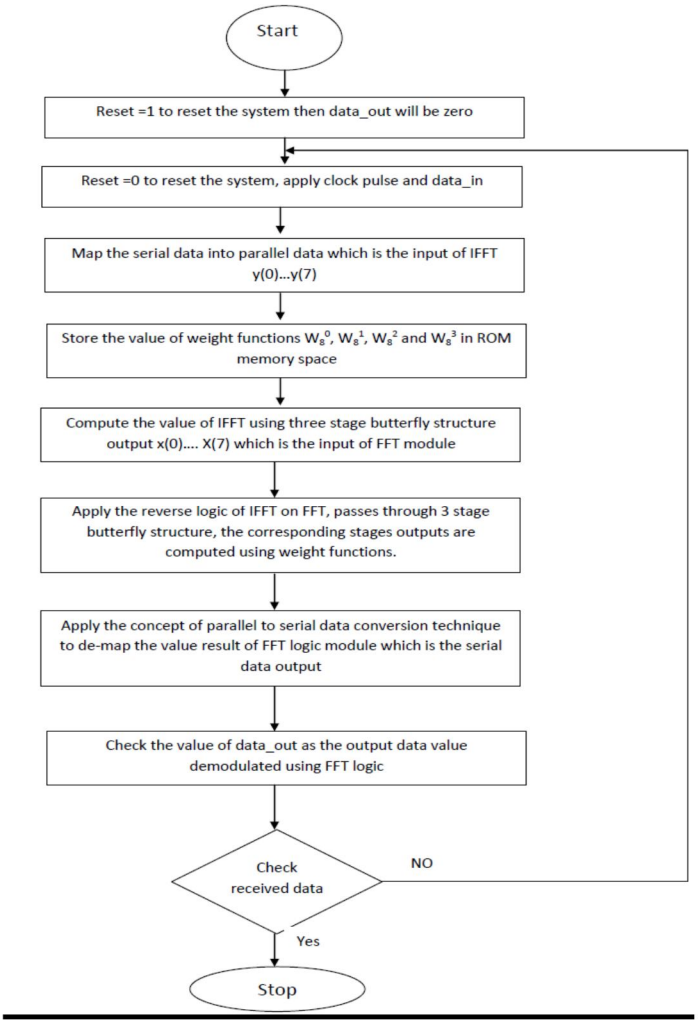


Fig. 7 flow diagram of 8-point FFT transreceiver

III. COMPARISON WITH IEEE PAPERS

Device utilization report is the report of used device hardware in the implementation of the chip and timing report is the minimum and maximum time to reach the output. Timing parameters are synchronized with the clock signal. Timing details provides the information of net delay, minimum period, minimum input arrival time before clock and maximum output required time after clock.

Table 5 comparative analysis of device utilization reference [2] and [10]

Device part	With IEEE Ref [2]	With IEEE Ref [10]	With Our design
Number of Slices	3007/72768 (4%)	14752/72768 (20%)	1775/72768 (3%)
Dedicated Logic Registers	4487/72768 (6%)	29504/72768 (40%)	2217/72768 (3%)
No of 4 input LUTs	4487/72768 (6%)	29504/72768 (40%)	2217/72768 (3%)
DSP Block elements	30/384 (8%)	24/384 (6%)	18/384 (5%)

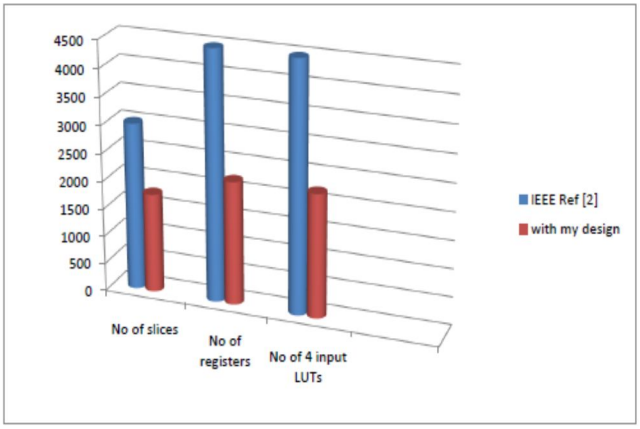


Fig. 8(a) comparison with ref [2] (Number of slices, LUTs and registers)

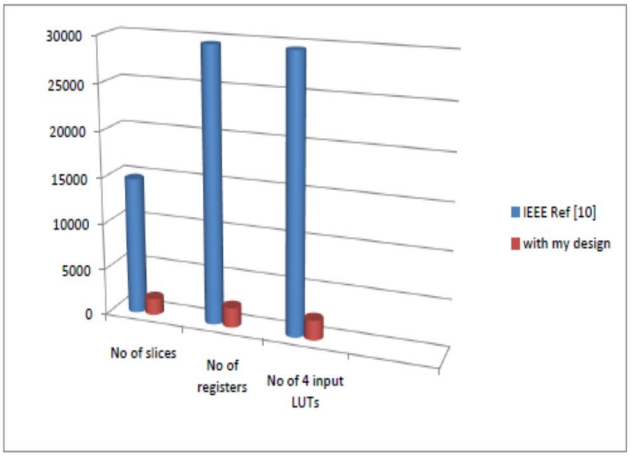


Fig. 8 (b) comparison with ref [10] (Number of slices, LUTs and registers)

The comparison charts of the design with IEEE ref [5] and IEEE ref [6] are shown in figure 8(a) and 8(b) respectively in terms of number of slices, number of 4 input LUTs and logic registers. Figure 8(c) is the combined graph comparing both papers and number of DSP elements are compared in the graph shown in the figure 8(d).

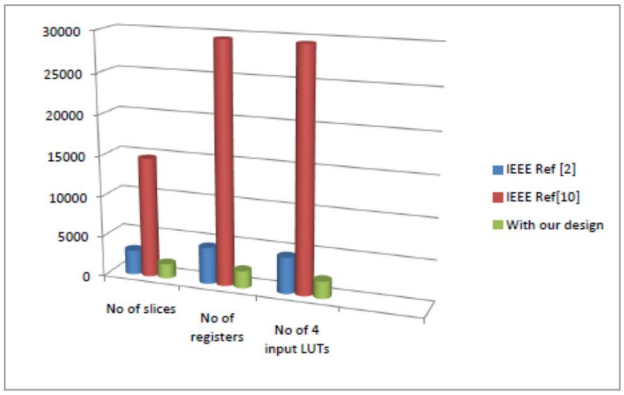


Fig. 8(c) comparison with ref [2] and ref [10]

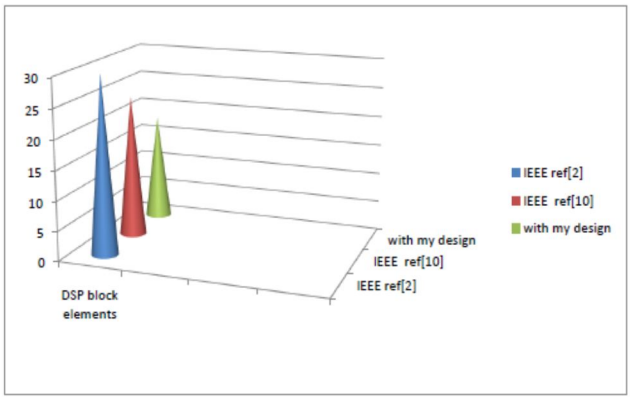


Fig. 8(d) Comparison with ref [2], ref [10] and with our design with respect to no. of DSP blocks

The data transfer of 64 bits is checked in terms of ASCII data format. The results of our simulation work compared with existing work with IEEE reference papers, ref [2] and ref [10]. In our design the number of slices utilization is 1775/72768 (3%), number of 4 input LUTs are 2117/72768 (3 %), number of registers 2117/72768 (3 %) and number of DSP blocks are 18. Our results are the optimized results with the existing work compared with existing IEEE papers. It is also seen that there is 17 % optimization in number of slices, 37 % in number of LUTs, 37 % in number of registers, 1 % in number of DSP blocks with ref [2] and 1 % optimization in number of slices, 3 % in number of LUTs, 3 % in number of registers, 1 % in number of DSP blocks with ref [10]. The results are the optimized solutions and applicable to extend the implementation for N variable FFT.

IV. CONCLUSION & FUTURE SCOPE

The hardware chip design and synthesis of variable FFT module is done on Xilinx 14.2 software with the help of VHDL programming language. The simulation results are tested on Modelsim 10.1 b student edition successfully. The FFT modules are tested for the different test cases. FFT is used in demodulation schemes and data transfer is checked out with FFT/IFFT transreceiver used in OFDM and OFDMA applications. The data transfer of 64 bits is checked in terms of ASCII data format. The results of our simulation work compared with existing work with IEEE reference papers, ref [2] and ref [10]. The design is applicable to develop 'N' point FFT. The feature of pipeline and parallel processing supports to execute the design upto 'N' points which are applicable to OFDMA applications.

The existing work can be used for Wimax and wireless technology in which fast computations are required. FFT implementation can be a good solution for multiple input multiple output (MIMO) system. So, it is possible to implement for MIMO OFDM and MIMO OFDMA systems. The robust high-bandwidth capabilities of orthogonal frequency division multiplexing (OFDM) confer immediate advantages on wireless products that can take advantage of it and many types of networking systems are doing so. OFDM underlies the existing IEEE 802.11 a wireless LAN (WLAN) standard and the proposed IEEE 802.11g WLAN standard, as well digital cable, digital TV, DSL, and power-line networking products. OFDM can also consider for use in 4G cellular systems.

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